

WHAT IS CLAIMED IS:

1. An improved CMOS image sensor wherein image lag at low light levels is reduced by controlling a reset level.
2. An improved CMOS image sensor wherein image quality is improved at low
5 light levels without compromising performance at high illumination by using a hard or soft reset dependent on signal level.
3. A CMOS image sensor with reduced image lag comprising:
an imaging device for acquiring image data;
a reset transistor for resetting the imaging device;
10 a readout transistor for providing pixel information as an output; and
a selection transistor for selecting between imaging devices, wherein image lag is reduced by controlling a reset level.
4. The CMOS image sensor of claim 3, wherein an amplifier gain setting is used to determine whether to use a hard reset or a soft reset.
- 15 5. The CMOS image sensor of claim 3, wherein the imaging device is a photodiode.
6. The CMOS image sensor of claim 3, wherein all transistors are of a same type.
7. The CMOS image sensor of claim 3, wherein the reset level is independent of a preceding signal level.
- 20 8. The CMOS image sensor of claim 3, wherein a drain of the reset transistor is connected to a voltage that is less than a supply voltage minus a threshold voltage.
9. The CMOS image sensor of claim 3, wherein a reset drain voltage can be switched between a supply voltage and a voltage that is less than the supply voltage minus a threshold voltage.

10. The CMOS image sensor of claim 3, wherein a reset drain level is determined by using gain of one color of pixel.

11. The CMOS image sensor of claim 3, wherein a reset drain level is determined by using a middle gain.

12. The CMOS image sensor of claim 3, wherein a reset drain level is changed only when gains of all color of pixels satisfy threshold conditions.

13. A CMOS image sensor with reduced image lag comprising:

an imaging device for acquiring image data;

a reset transistor for resetting the imaging device;

a readout transistor for providing pixel information as an output; and

a selection transistor for selecting between imaging devices, wherein image lag is reduced by controlling a reset level which is switchable between a supply voltage and a supply voltage minus a threshold voltage of the reset transistor.

14. The CMOS image sensor of claim 13, wherein an amplifier gain setting is used to determine whether to use a hard reset or a soft reset.

15. The CMOS image sensor of claim 13, wherein the imaging device is a photodiode.

16. The CMOS image sensor of claim 13, wherein all transistors are of a same type.

17. The CMOS image sensor of claim 13, wherein the reset level is independent of a preceding signal level.

18. The CMOS image sensor of claim 13, wherein a drain of the reset transistor is connected to a voltage that is less than a supply voltage minus a threshold voltage.

19. The CMOS image sensor of claim 13, wherein a reset drain voltage can be switched between a supply voltage and a voltage that is less than the supply voltage

minus a threshold voltage.

20. The CMOS image sensor of claim 13, wherein a reset drain level is determined by using gain of one color of pixel.

21. The CMOS image sensor of claim 13, wherein a reset drain level is determined
5 by using a middle gain.

22. The CMOS image sensor of claim 13, wherein a reset drain level is changed only when gains of all color of pixels satisfy threshold conditions.